CLAIMS

Please reconsider the pending claims as set forth below in view of the IDS accompanying this RCE . A listing of all pending claims is presented below.

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Previously Presented) A semiconductor device comprising:

a p-channel type field effect transistor and an n-channel type field effect transistor both formed in a semiconductor layer which has a strain effect and which is formed in an upper layer of a semiconductor substrate,

wherein a source/a drain of said p-channel type field effect transistor and a source/a drain of said n-channel type field effect transistor are formed only in said semiconductor layer having the strain effect,

wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect, and

wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

10. (Canceled)

11. (Previously Presented) A semiconductor device according to claim 9, wherein each of said p-channel type field effect transistor and said n-channel type field effect transistor comprises:

silicon epitaxial layers formed on said source/drain; and

refractory metal silicide layers formed on said silicon epitaxial layers.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Cancelled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Previously Presented) A semiconductor device according to claim 9, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Previously Presented) A semiconductor device, comprising

a semiconductor substrate having a buffer layer on a silicon base layer, wherein the buffer layer is made of a $P^-$ type silicon germanium,

a relax layer on the buffer layer, wherein the relax layer is made of P type silicon germanium which is relaxed, and

a silicon strain effect layer on the relax layer;

a gate electrode of a p-channel type field effect transistor and a gate electrode of a n-channel type field effect transistor on said strain effect silicon layer through a gate insulating film;

a source and a drain each composed of p-type diffusion layer only in said silicon strain effect layer on both sides of said gate electrode of said p-channel type field effect transistor, the source and drain of the p-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

a source and a drain each composed of n-type diffusion layer only in said strain effect silicon layer on both sides of said gate electrode of said n-channel type field effect transistor, the source and drain of the n-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer; and

an isolation region in between the p-channel type field effect transistor and the n-channel type field effect transistor in said strain effect silicon layer.

30. (Previously Presented) The semiconductor device according to claim 29, wherein the buffer layer is constructed of $Si_{1-x}Ge_x$, wherein a concentration of germanium of the buffer layer changes from X=0.04 to X=0.3 from a side of the buffer layer opposite to the relax layer to a side of the buffer layer proximate the relax layer.

31. (Previously Presented) The semiconductor according to claim 29, wherein the relax layer is formed of $Si_{1-x}Ge_x$, wherein a concentration of germanium of the relax layer is X=0.3.

32. (Previously Presented) A semiconductor device, comprising:

a semiconductor substrate having a silicon layer having a strain effect in an upper layer of said semiconductor substrate, a relax layer below the silicon layer having the strain effect, and a buffer layer below the relax layer;

a gate electrode of a p-channel type field effect transistor on said strain effect silicon layer through a gate insulating film;

a source and a drain each composed of p-type diffusion in only said strain effect silicon layer on both sides of said gate electrode of said p-channel type field effect transistor, the source and drain of the p-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

a source and a drain each composed of n-type diffusion layer in only said strain effect silicon layer on both sides of a gate electrode of an n-channel type field effect transistor, the source and drain of the n-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

an isolation region in between the p-channel type field effect transistor and the n-channel type field effect transistor in said silicon layer having the strain effect;

and

wherein the buffer layer is constructed of a $P^-$ type silicon germanium, wherein the relax layer is made from a $P^-$ type silicon germanium whose stress is relaxed.

33. (Previously Presented) The semiconductor device of claim 32, wherein the semiconductor substrate includes:

the buffer layer located on a silicon base layer;

a relax layer on the buffer layer; and

the silicon stain effect layer on the relax layer on the buffer layer.

34. (Previously Presented) The semiconductor of claim 33, wherein the relax layer is formed of n-type silicon germanium.

35. (Cancelled)

36. (Previously Presented) The semiconductor of claim 32, wherein a semiconductor substrate having the strain effect silicon layer causes the strain effect silicon layer to exhibit a strain effect in the range of 5 nm to 30 nm.

37. (Previously Presented) The semiconductor according to claim 32, wherein the buffer layer is constructed of $Si_{1-x}Ge_x$, wherein a concentration of germanium of the buffer layer proximate the relax layer changes from X=0.04 to X=0.3 from a side of the buffer layer proximate the relax layer.

38. (Previously Presented) The semiconductor according to claim 32, wherein the relax layer is formed of Si1-xGex3 wherein a concentration of germanium of the relax layer is X=0.3.